In the Specification

Please replace paragraphs [0022]-[0025] with the following:

[0022] ~~The~~ In one aspect, the invention provides an interleaved clock generator that generates *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer. The interleaved clock generator comprises an interleaved clock generator of a first type for receiving the input clock signal and for generating *M* interleaved intermediate clock signals in response to the input clock signal, where *M* is a factor of *N* and is an integer greater than unity. The interleaved clock generator of the first type includes either a multi-stage serial-delay circuit or a ring counter circuit. The interleaved clock generator additionally comprises *M* interleaved clock generators of a second type, each of which is each for receiving a respective one of the intermediate clock signals from the clock generator of the first type and for generating N/M of the *N* interleaved clock signals in response to the respective one of the intermediate clock signals. Each of the interleaved clock generators of the second type includes either a ring counter circuit or a multi-stage serial-delay circuit: a ring counter when the interleaved clock generator of the first type includes a multi-stage serial-delay circuit; a multi-stage serial-delay circuit when the interleaved clock generator of the first type includes a ring counter circuit. In the clock generator, corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td; the interleaved clock signals have a frequency of 1/(N*Td); the input clock signal has a frequency of 1/(M*Td) when the interleaved clock generator of the first type includes the multi-stage serial delay circuit; and the input clock signal has a frequency of M/(N*Td) when the interleaved clock generator of the first type includes the ring counter circuit.

[0022A] In another aspect, the invention provides an interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer. The interleaved clock generator comprises an interleaved clock generator of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N*

and is an integer greater than unity. The interleaved clock generator means of the first type includes a multi-stage serial-delay circuit. The interleaved clock generator also comprises *M* interleaved clock generators of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals. Each of the interleaved clock generator means of the second type includes a ring counter circuit. In the interleaved clock generator, the input clock signal comprises differential clock signals each having a 50% duty cycle; and the multi-stage serial-delay circuit includes M/2 delay stages, each providing two of the intermediate clock signals.

[0022B] In another aspect, the invention provides an interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer. The interleaved clock generator comprises an interleaved clock generator of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity. The interleaved clock generator of the first type includes a ring counter circuit. The interleaved clock generator additionally comprises *M* interleaved clock generators of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator of the first type and for generating in response thereto N/M of the *N* interleaved clock signals. Each of the interleaved clock signal generators of the second type includes a multi-stage serial-delay circuit.

[0023] In another aspect, the ~~The~~ invention also provides an interleaved clock generator that generates *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer. The interleaved clock generator comprises an interleaved clock generator of a first type and *M* interleaved clock generators of a second type, where *M* is a factor of *N* and is an integer greater than unity. The interleaved clock generator of the first type includes a clock input connected to receive the input clock signal, *M* intermediate clock outputs and either a multi-stage serial-delay circuit or a ring counter

circuit. The interleaved clock generator of the first type operates in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs.

[0024] Each of the *M* interleaved clock generators of the second type includes an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and either a ring counter circuit or a multi-stage serial-delay circuit. The interleaved clock signal generator of the second type includes a ring counter in an embodiment in which the interleaved clock generator of the first type includes a multi-stage serial-delay circuit, and includes a multi-stage serial-delay circuit in an embodiment in which the interleaved clock generator of the first type includes a ring counter circuit. Each of the interleaved clock generators of the second type operates in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs. In the clock generator, corresponding edges of temporally adjacent ones of the interleaved clock signals differ in time by a time delay Td; the interleaved clock signals have a frequency of 1/(N×Td); the input clock signal has a frequency of 1/(M×Td) when the interleaved clock generator of the first type includes the multi-stage serial delay circuit; and the input clock signal has a frequency of M/(N×Td) when the interleaved clock generator of the first type includes the ring counter circuit.

[0024A] In another aspect, the invention provides an interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer. The interleaved clock generator comprises an interleaved clock generator of a first type, including a clock input connected to receive the input clock signal, *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity, and a ring counter circuit. The interleaved clock generator of the first type operates in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs. The interleaved clock generator additionally comprises *M* interleaved clock generators of a second type, each including

an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and a multi-stage serial-delay circuit. Each of the interleaved clock generators of the second type operates in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs multi-stage serial-delay circuit.

[0024B] In another aspect, the invention provides an interleaved clock generator for generating N interleaved clock signals in response to an input clock signal, where N is a non-prime integer. The interleaved clock generator comprises a multi-stage serial-delay circuit connected to receive the input clock signal, the multi-stage serial-delay circuit including M intermediate clock outputs where M is a factor of N and is an integer greater than unity; and connected to each of the M intermediate clock outputs, a ring counter circuit that generates N/M of the N interleaved clock signals. In the interleaved clock generator, corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td; the interleaved clock signals have a frequency of 1/(N*Td); and the input clock signal has a frequency of 1/(M*Td).

[0025] Finally, the invention provides an interleaved clock generator that generates *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer. The interleaved clock generator comprises a multi-stage serial-delay circuit. The multi-stage serial-delay circuit is connected to receive the input clock signal and includes M intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity. The interleaved clock generator additionally comprises a ring counter circuit connected each of the M intermediate clock outputs. The ring counter circuit generates N/M of the *N* interleaved clock signals. In the interleaved clock generator, corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td; the interleaved clock signals have a frequency of 1/(N*Td); and the input clock signal has a frequency of 1/(M*Td).